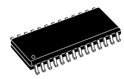
TDA7468

TWO BANDS DIGITALLY CONTROLLED AUDIO PROCESSOR WITH BASS ALC SURROUND

1 FEATURES

- INPUT MULTIPLEXER
  - 4 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- BASS ALC
- TREBLE AND BASS CONTROL IN 2.0dB
- STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA
- SERIAL BUS
- EXTERNALLY ADJUSTABLE SURROUND

Figure 1. Package



SO28

Table 1. Order Codes

Part Number	Package
TDA7468D	SO28
TDA7468D13TR	Tape & Reel

2 DESCRIPTION

The TDA7468D is a volume tone (bass and treble) balance (Left/Right) processor for quality audio applications in Hi-Fi systems.

Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained

Figure 2. PIN CONNECTION (Top view)

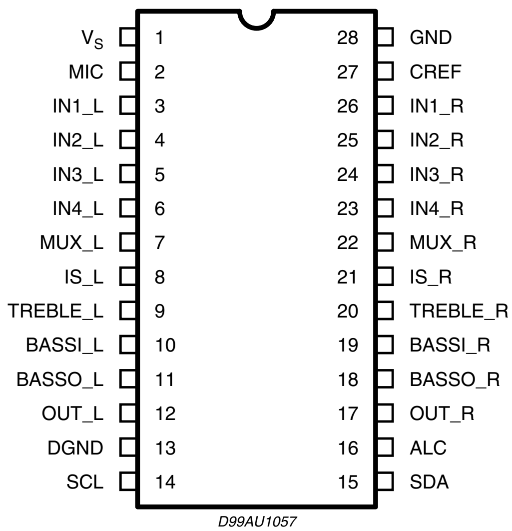


Figure 3. BLOCK DIAGRAM

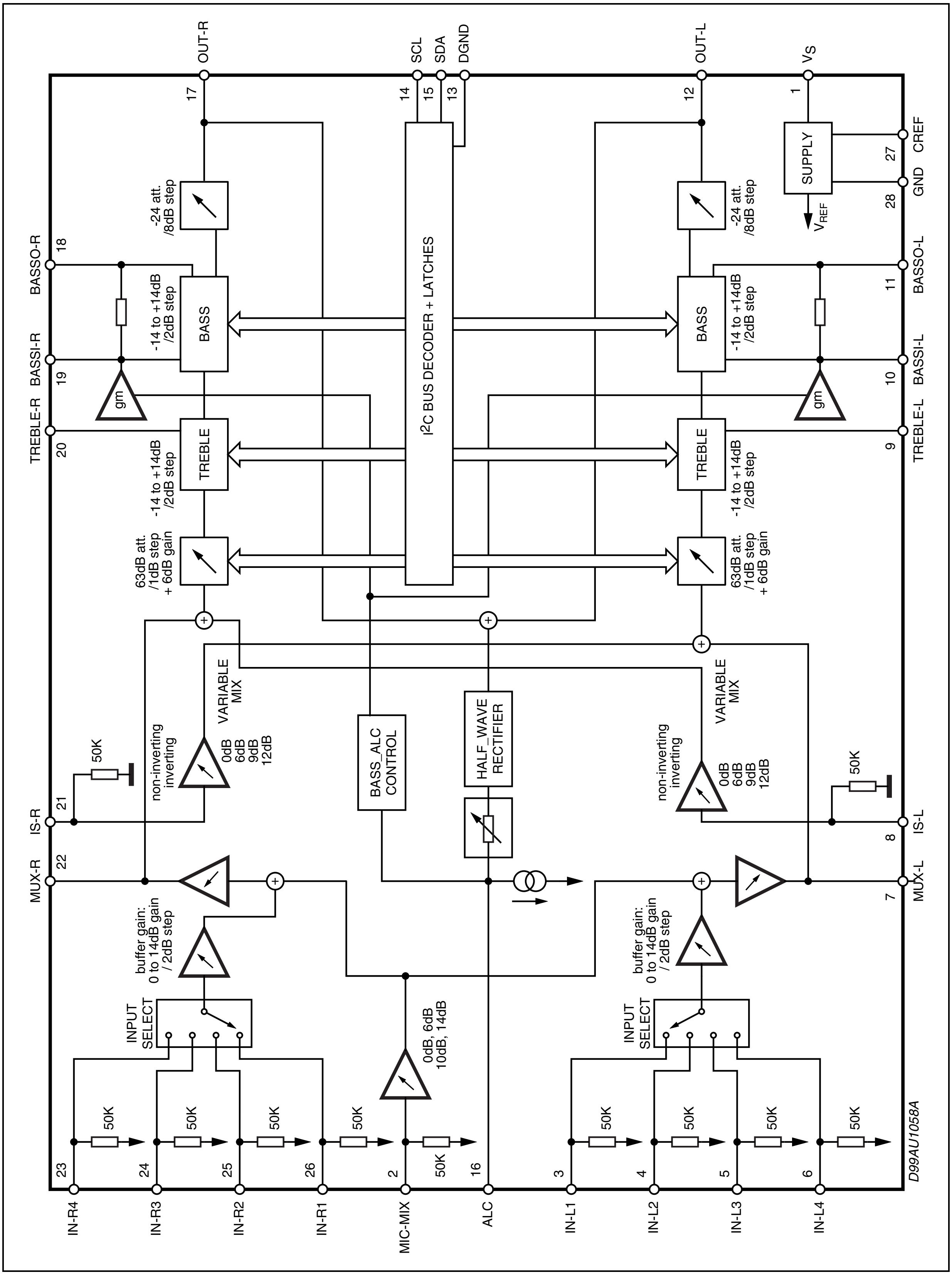


Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Table 3. THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	Thermal Resistance Junction-pins	85	°C/W

Table 4. QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	5	9	10	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V_I = 1Vrms; f = 1KHz		0.01	%	%
	Total Harmonic Distortion V_I = 0.1Vrms; f = 1KHz			0.1	%
S/N	Signal to Noise Ratio V_{out} = 1Vrms (0dB)		100		dB
S_C	Channel Separation f = 1KHz		90		dB
	Input Gain (2dB step)	0		14	dB
	Volume Control (1dB step)	-87		0	dB
	Treble Control (2dB step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Mute Attenuation		86		dB

ELECTRICAL CHARACTERISTICS

(refer to the test circuit T_{amb} = 25°C, V_S = 9V, f = 1KHz all controls flat (G = 0dB), unless otherwise specified)

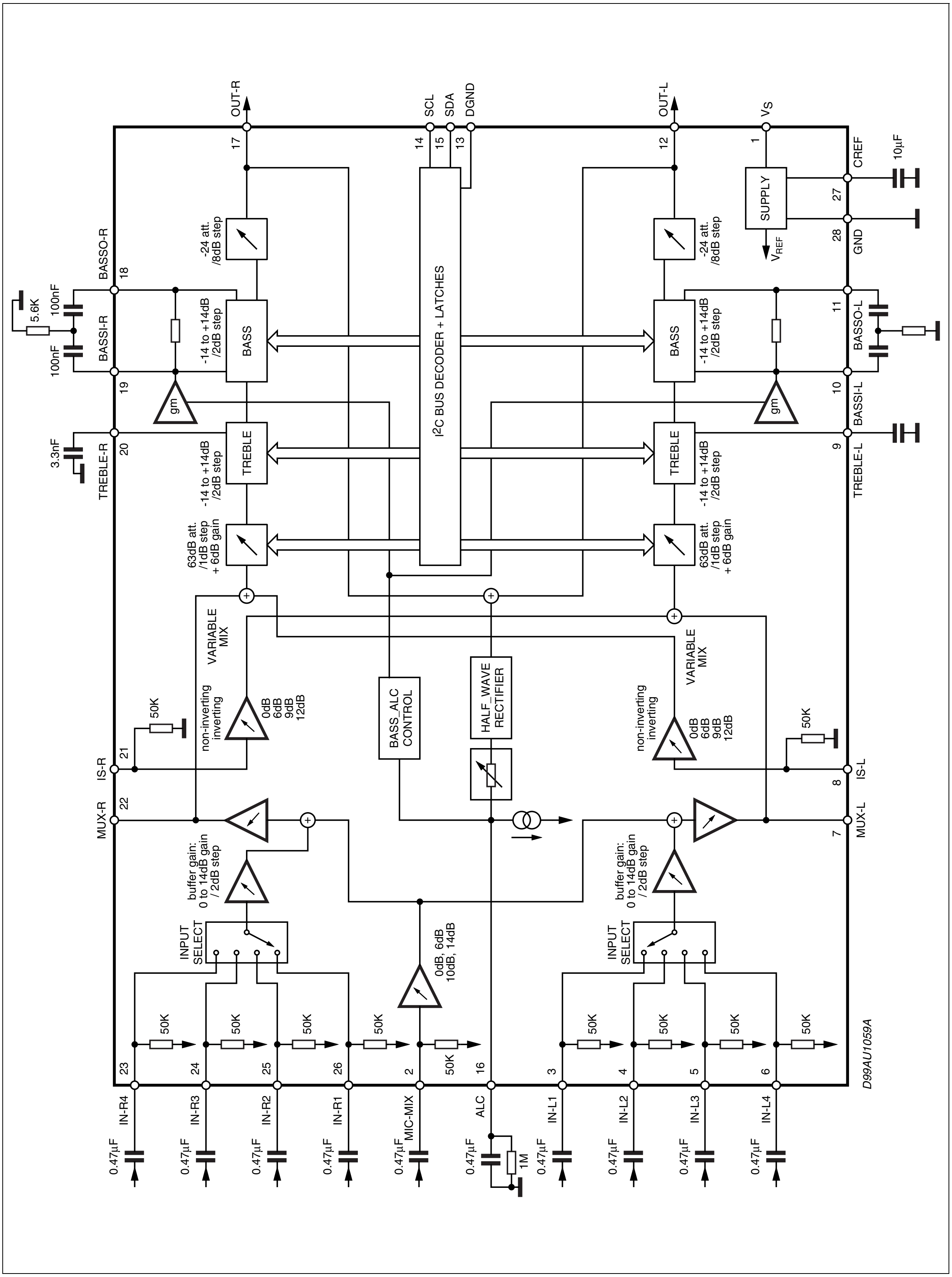
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		5	9	10	V
I_S	Supply Current			9		mA
SVR	Ripple Rejection		60	90		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		V_{rms}
S_{IN}	Input Separation		80	100		dB
G_{inmin}	Minimum Input Gain		-1	0	1	dB
G_{inmax}	Maximum Input Gain			14		dB
G_{step}	Step Resolution			2		dB
MIC						
R_{IN}	Input Resistance		35	50	65	KΩ
G_{mic1}	Mic Input Gain 1			14		dB
G_{mic2}	Mic Input Gain 2			10		dB
G_{mic3}	Mic Input Gain 3			6		dB
G_{min4}	Mic Input Gain 4			0		dB
MIX_{mic}	Mixing Rate			50		%
SURROUND						
R_{in}	Input Resistance		35	50	65	KΩ
G_{inmin}	Minimum Input Gain		-1	0	1	dB
G_{inmax}	Maximum Input Gain			12		dB
G_{inV}	Inverting Gain			-1		
M_{ixmin}	Minimum Mixing Rate			0		%
M_{ixmax}	Maximum Mixing Rate			100		%
Crosstalk	Crosstalk of Mux Output to 100% IS		40			dB
G_{buffer}	Buffer Gain			6		dB
VOLUME CONTROL						
C_{RANGE1}	Vol 1 Control Range			63		dB
A_{VMAX1}	Vol 1 Max. Attenuation		61	63	65	dB
A_{STEP1}	Vol 1 Step Resolution		0.5	1	1.5	dB
Match1	Matching			TBD		dB
C_{RANGE2}	Vol 2 Control Range			24		dB
A_{VMAX2}	Vol 2 Max. Attenuation		22	24	26	dB
A_{STEP2}	Vol 2 Step Resolution		7	8	9	dB
Match2	Matching			TBD		dB
A_{VMAX1}+ A_{VMAX2}	Vol 1 + Vol 2 Max Attenuation			84		dB

ELECTRICAL CHARACTERISTICS (continua)

(refer to the test circuit T_{amb} = 25°C, V_S = 9V, f = 1KHz all controls flat (G = 0dB), unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BASS CONTROL						
Gb	Control Range	Max. Boost/cut	±12.0	±14.0	±16.0	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		33	44	55	KΩ
BASS ALC CONTROL						
$R_{attack1}$	Attack Time Resistor 1			12.5		KΩ
$R_{attack2}$	Attack Time Resistor 2			25		KΩ
$R_{attack3}$	Attack Time Resistor 3			50		KΩ
$R_{attack4}$	Attack Time Resistor 4			100		KΩ
Thresh1	Threshold 1			700		mVrms
Thresh2	Threshold 2			485		mVrms
Thresh3	Threshold 3			320		mVrms
Thresh4	Threshold 4			170		mVrms
TREBLE CONTROL						
Gt	Control Range	Max. Boost/cut	+13.0	+14.0	+15.0	dB
T_{STEP}	Step Resolution		1	2	3	dB
R_t	Internal Resistance			25		KΩ
AUDIO OUTPUTS						
V_{OCL}	Clipping Level	THD = 0.3%	2	2.5		V_{rms}
R_L	Output Load Resistance		2			KΩ
VO_{UT}	DC Voltage Level			4.5		V
GENERAL						
E_{NO}	Output Noise	BW = 20Hz to 20KHz;				
		All gains 0dB;				
		output muted		5		µV
		flat		10	15	µV
S/N	Signal to Noise Ratio	All gains 0dB; V_O = 1V_{rms} ;		100		dB
S_C	Channel Separation Left/Right			90		dB
d	Distortion	A_V = 0; V_I = 0.1V_{rms} ;			0.1	%
		A_V = 0; V_I = 1V_{rms} ;		0.01		%
S_C	Channel Separation left/right			90		dB
	Total Tracking Error			0	1	dB
BUS INPUT						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		2.5			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage (ACK)	I_O = 1.6mA		0.4	0.8	V

Figure 4. TEST CIRCUIT



3 APPLICATION SUGGESTIONS

The first and the last stages are volume control blocks. The control range is 0 to -63dB (mute) with 1dB step resolution for this first one, 0 to 24dB (mute) with 8dB step resolution for the last one.

The very high resolution allows the implementation of systems free from any noisy acoustical effect.

The TDA7468D audioprocessor provides 2 bands tones control.

3.1 Bass, Stages

The Bass cell has an internal resistor R_i = 44KΩ typical.

Several filter types can be implemented, connecting external components to the Bass IN and OUT pins.

The fig.5 refers to basic T Type Bandpass Filter starting from the filter component values (R1 internal and R2,C1,C2 external) the centre frequency Fc, the gain Av at max. boost and the filter Q factor are computed as follows:

$$F_C = \frac{1}{2 \cdot \pi \cdot \sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}$$

$$A_V = \frac{R2\ C2 + R2\ C1 + Ri\ C1}{R2\ C1 + R2\ C2}$$

$$Q = \frac{\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}{R2\ C1 + R2\ C2}$$

Viceversa, once F_C, A_V, and R_i internal value are fixed, the external components values will be:

$$C1 = \frac{A_V - 1}{2 \cdot \pi \cdot F_C \cdot R_i \cdot Q} \qquad C2 = \frac{Q^2 \cdot C1}{A_V - 1 - Q^2}$$

$$R2 = \frac{A_V - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot F_C \cdot (A_V - 1) \cdot Q}$$

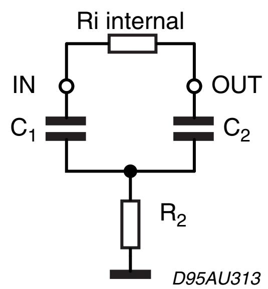
3.2 Treble Stage

The treble stage is a high pass filter whose time constant is fixed by an internal resistor (25KΩ typical) and an external capacitor connected between treble pins and ground.

3.3 CREF

The suggested 10µF reference capacitor (CREF) value can be reduced to 4.7µF if the application requires faster power ON.

Figure 5.



4 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7468D and vice versa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

4.1 Data Validity

As shown in fig. 6, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

4.2 Start and Stop Conditions

As shown in fig.7 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

4.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

4.4 Acknowledge

The master (µP) puts a restive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 4). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse. The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

4.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking.

Figure 6. Data Validity on the I²CBUS

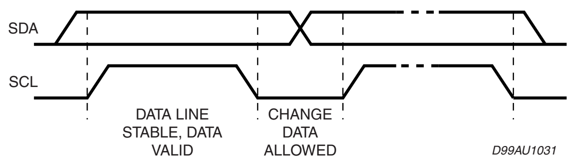


Figure 7. Timing Diagram of I²CBUS

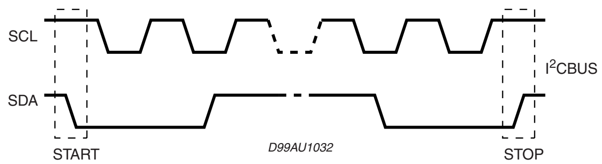
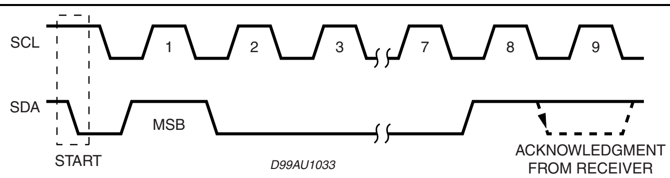


Figure 8. Acknowledge on the I²CBUS



5 SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7468D address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

	CHIP ADDRESS									SUBADDRESS						DATA 1 to DATA n								
	MSB							LSB		MSB			LSB			MSB						LSB		
S	1	0	0	0	1	0	0	0	ACK	X	X	X	B	DATA	ACK				DATA				ACK	P

D96AU420

ACK = Acknowledge

S = Start; P = Stop

A = Address

B = Auto Increment

6 EXAMPLES

6.1 No Incremental Bus

The TDA7468D receives a start condition, the correct chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.

	CHIP ADDRESS									SUBADDRESS									DATA								
	MSB							LSB		MSB							LSB		MSB						LSB		
S	1	0	0	0	1	0	0	0	ACK	X	X	X	0	D3	D2	D1	D0	ACK				DATA				ACK	P

D96AU421

6.2 Incremental Bus

The TDA7468D receive a start conditions, the correct chip address, a subaddress with the B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receivers the stop condition.

	CHIP ADDRESS									SUBADDRESS									DATA 1 to DATA n								
	MSB							LSB		MSB							LSB		MSB						LSB		
S	1	0	0	0	1	0	0	0	ACK	X	X	X	1	D3	D2	D1	D0	ACK				DATA				ACK	P

D96AU422

Table 5. POWER ON RESET CONDITION

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	1	1	1	1	1	0

7 DATA BYTES

Address = (HEX) 10001000.

Table 6. FUNCTION SELECTION: First byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT SELECT & MIC
X	X	X	B	0	0	0	1	INPUT GAIN
X	X	X	B	0	0	1	0	SURROUND
X	X	X	B	0	0	1	1	VOLUME LEFT
X	X	X	B	0	1	0	0	VOLUME RIGHT
X	X	X	B	0	1	0	1	TREBLE & BASS
X	X	X	B	0	1	1	0	OUTPUT
X	X	X	B	0	1	1	1	BASS ALC

B = 1: INCREMENTAL BUS; ACTIVE
B = 0: NO INCREMENTAL BUS
X = INDIFFERENT 0/1

Table 7. INPUT SELECTION & MIC

MSB							LSB	
D7	D6	D5	D4	D3	D2	D1	D0	
								INPUT SELECT
					0	0	0	IN1
					0	0	1	IN2
					0	1	0	IN3
					0	1	1	IN4
								MUTE (IN5)
					1			ON (IN5)
					0			OFF
								MIC
			0	0				Gain: 14dB
			0	1				Gain: 10dB
			1	0				Gain: 6dB
			1	1				Gain: 0dB
		1						OFF
		0						ON

Table 8. INPUT GAIN SELECTION

MSB							LSB	INPUT GAIN
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
					0	0	0	0dB
					0	0	1	2dB
					0	1	0	4dB
					0	1	1	6dB
					1	0	0	8dB
					1	0	1	10dB
					1	1	0	12dB
					1	1	1	14dB

GAIN = 0 to 30dB

Table 9. SURROUND

MSB							LSB	SURROUND
D7	D6	D5	D4	D3	D2	D1	D0	
								SURROUND MODE
							1	ON
							0	OFF
								GAIN
					0	0		0dB
					0	1		6dB
					1	0		9dB
					1	1		12dB
								MIXING
		0	0	0				inverting : 100%
		0	0	1				inverting :50%
		0	1	0				inverting : 25%
		0	1	1				0%
		1	0	0				non-inverting : 100%
		1	0	1				non-inverting : 75%
		1	1	0				non-inverting : 50%
		1	1	1				mute
								BUFFER GAIN
	1							0
	0							6dB

Table 10. VOLUME

MSB							LSB	VOLUME
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**1dB STEPS**
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
								8dB STEPS
		0	0	0				0dB
		0	0	1				-8dB
		0	1	0				-16dB
		0	1	1				-24dB
		1	0	0				-32dB
		1	0	1				-40dB
		1	1	0				-48dB
		1	1	1				-56dB
								VOLUME 2
0	0							0dB
0	1							-8dB
1	0							-16dB
1	1							-24dB

VOLUME = 0 to-87dB

Table 11. VOLUME setting 1

Target Volume (dB)	Volume1 1dB step (dB)	Volume1 8dB step (dB)	Volume2 8dB step (dB)
0	0	0	0
-1	-1		
-2	-2		
-3	-3		
-4	-4		
-5	-5		
-6	-6		
-7	-7		
-8	0	-8	0
-9	-1		
-10	-2		
-11	-3		
-12	-4		
-13	-5		
-14	-6		
-15	-7		

Table 11. VOLUME setting 1 (continua)

Target Volume (dB)	Volume1 1dB step (dB)	Volume1 8dB step (dB)	Volume2 8dB step (dB)
-16	0	-16	0
-17	-1		
-18	-2		
-19	-3		
-20	-4		
-21	-5		
-22	-6		
-23	-7		
-24	0	-24	0
-25	-1		
-26	-2		
-27	-3		
-28	-4		
-29	-5		
-30	-6		
-31	-7		
-32	0	-32	0
-33	-1		
-34	-2		
-35	-3		
-36	-4		
-37	-5		
-38	-6		
-39	-7		
-40	0	-40	0
-41	-1		
-42	-2		
-43	-3		
-44	-4		
-45	-5		
-46	-6		
-47	-7		
-48	0	-48	0
-49	-1		
-50	-2		
-51	-3		
-52	-4		
-53	-5		
-54	-6		
-55	-7		
Target Volume (dB)	Volume1 1dB step (dB)	Volume1 8dB step (dB)	Volume2 8dB step (dB)
-56	0	-56	0
-57	-1		

Table 11. VOLUME setting 1 (continua)

-58	-2		
-59	-3		
-60	-4		
-61	-5		
-62	-6		
-63	-7		
-64	0	-56	8
-65	-1		
-66	-2		
-67	-3		
-68	-4		
-69	-5		
-70	-6		
-71	-7		
-72	0	-56	-16
-73	-1		
-74	-2		
-75	-3		
-76	-4		
-77	-5		
-78	-6		
-79	-7		
-80	0	-56	-24
-81	-1		
-82	-2		
-83	-3		
-84	-4		
-85	-5		
-86	-6		
-87	-7		

Table 12. VOLUME setting 2

Target Volume (dB)	Volume1 1dB step (dB)	Volume1 8dB step (dB)	Volume2 8dB step (dB)
0	0	0	0
-1	-1		
-2	-2		
-3	-3		
-4	-4		
-5	-5		
-6	-6		
-7	-7		

Table 12. VOLUME setting 2 (continua)

Target Volume (dB)	Volume1 1dB step (dB)	Volume1 8dB step (dB)	Volume2 8dB step (dB)
-8	0	-8	0
-9	-1		
-10	-2		
-11	-3		
-12	-4		
-13	-5		
-14	-6		
-15	-7		
-16	0	-16	0
-17	-1		
-18	-2		
-19	-3		
-20	-4		
-21	-5		
-22	-6		
-23	-7		
-24	0	-16	-8
-25	-1		
-26	-2		
-27	-3		
-28	-4		
-29	-5		
-30	-6		
-31	-7		
-32	0	-16	-16
-33	-1		
-34	-2		
-35	-3		
-36	-4		
-37	-5		
-38	-6		
-39	-7		
-40	0	-16	-24
-41	-1		
-42	-2		
-43	-3		
-44	-4		
-45	-5		
-46	-6		
-47	-7		

Table 12. VOLUME setting 2 (continua)

Target Volume (dB)	Volume1 1dB step (dB)	Volume1 8dB step (dB)	Volume2 8dB step (dB)
-48	0	-24	-24
-49	-1		
-50	-2		
-51	-3		
-52	-4		
-53	-5		
-54	-6		
-55	-7		
-56	0	-32	-24
-57	-1		
-58	-2		
-59	-3		
-60	-4		
-61	-5		
-62	-6		
-63	-7		
-64	0	-40	-24
-65	-1		
-66	-2		
-67	-3		
-68	-4		
-69	-5		
-70	-6		
-71	-7		
-72	0	-48	-24
-73	-1		
-74	-2		
-75	-3		
-76	-4		
-77	-5		
-78	-6		
-79	-7		
-80	0	-56	-24
-81	-1		
-82	-2		
-83	-3		
-84	-4		
-85	-5		
-86	-6		
-87	-7		

Table 13. TREBLE & BASS SELECTION

MSB							LSB	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**TREBLE**
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	0	0	0	14dB
				1	0	0	1	12dB
				1	0	1	0	10dB
				1	0	1	1	8dB
				1	1	0	0	6dB
				1	1	0	1	4dB
				1	1	1	0	2dB
				1	1	1	1	0dB
								BASS (*)
0	0	0	0					-14dB
0	0	0	1					-12dB
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					0dB
1	0	0	0					14dB
1	0	0	1					12dB
1	0	1	0					10dB
1	0	1	1					8dB
1	1	0	0					6dB
1	1	0	1					4dB
1	1	1	0					2dB
1	1	1	1					0dB

(*) When BASS is programmed in the range -14dB/0dB, ALC is automatically switched to "OFF".

Table 14. OUTPUT

MSB							LSB	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**MUTE**
							0	ON
							1	OFF

Table 15. BASS ALC

MSB							LSB	BASS ALC
D7	D6	D5	D4	D3	D2	D1	D0	
								ALC Mode
							1	ON
							0	OFF
								Detector
						1		ON
						0		OFF
								Release Current Circuit
					1			ON
					0			OFF
								Attack Time Resistor
			0	0				12.5KΩ
			0	1				25KΩ
			1	0				50KΩ
			1	1				100KΩ
								Threshold
	0	0						700mVrms
	0	1						485mVrms
	1	0						320mVrms
	1	1						170mVrms
								Attack Mode
0								MODE 1: Fixed Resistor
1								MODE 2: Adaptive

Figure 9. BASS ALC : Threshold curve

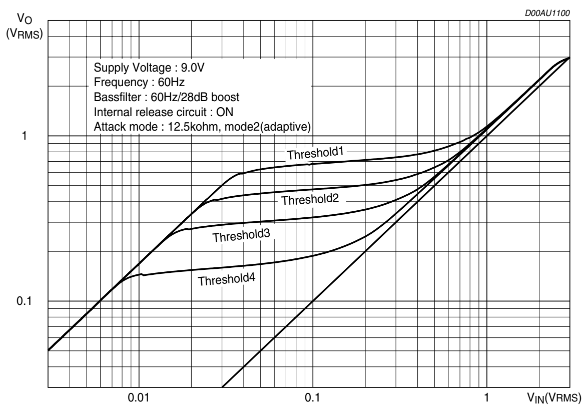
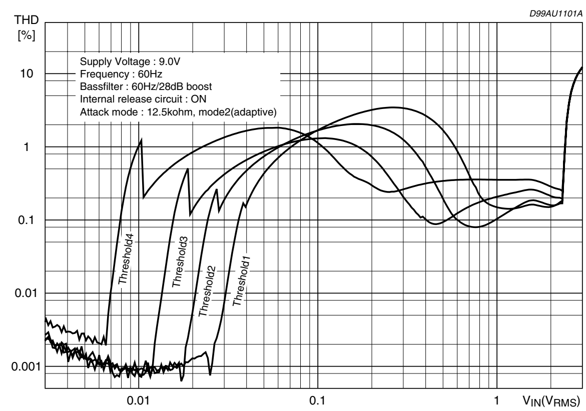


Figure 10. BASS ALC : THD



8 IC1

Figure 11. PINS: IN1_L, IN1_R, IN2_L, IN2_R, IN3_L, IN3_R, IN4_L, IN4 _R, IS_L, IS_R, MIC

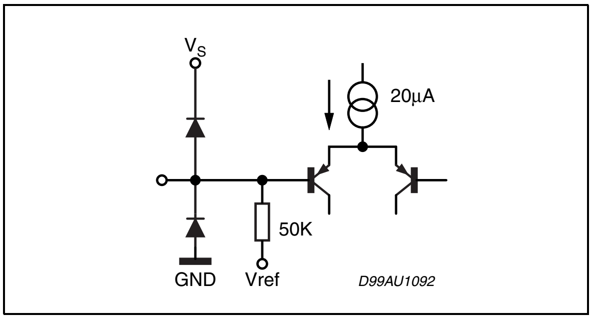


Figure 12. PINS: OUT_L, OUT_R, IMUX_L, MUX_R

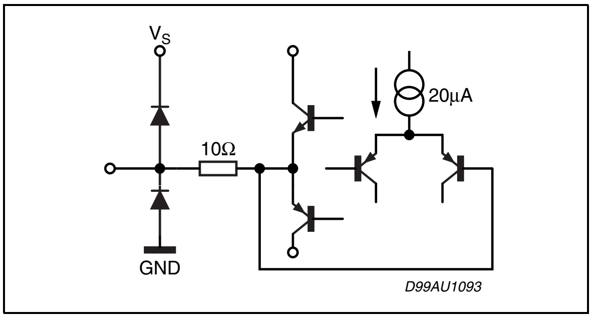


Figure 13. PINS: TREBLE_L, TREBLE_R

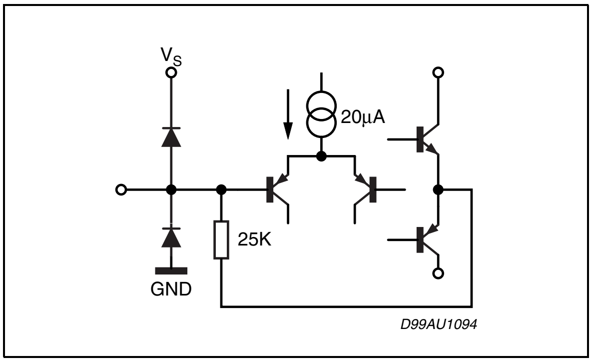


Figure 14. PINS: SCL, SDA

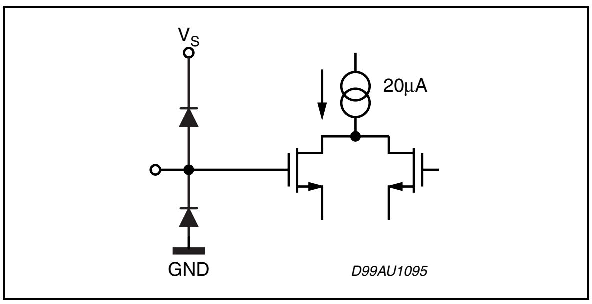


Figure 15. PINS: BASSI_L, BASSI_R

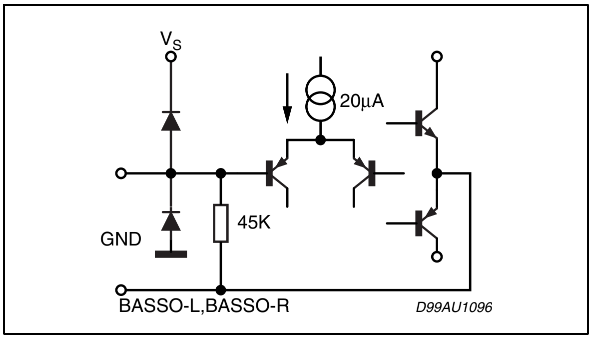


Figure 16. PINS: BASSO_L, BASSO_R

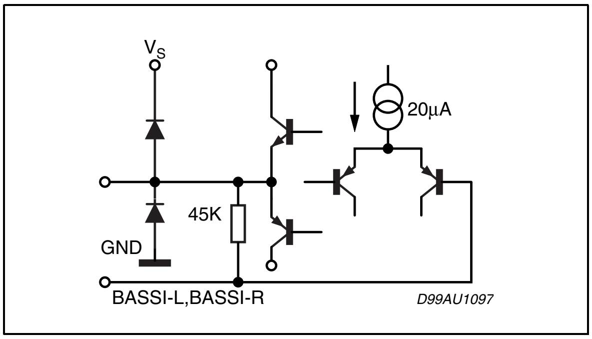


Figure 17. PIN: ALC

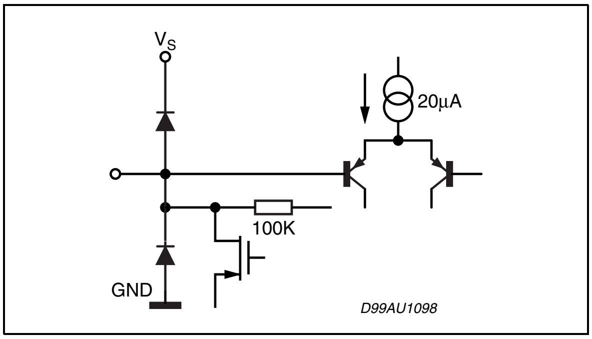
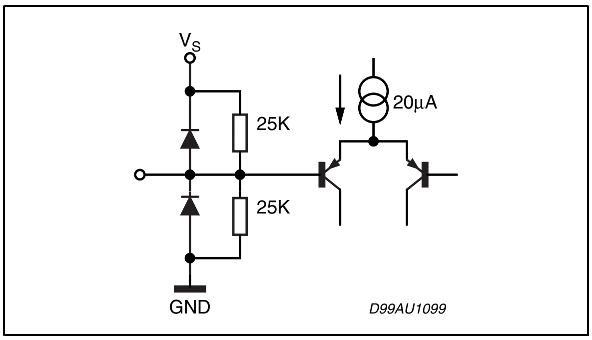


Figure 18. PIN: CREF



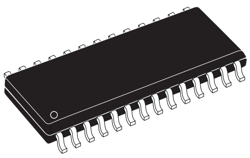
9 PACKAGE MECHANICAL DATA

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

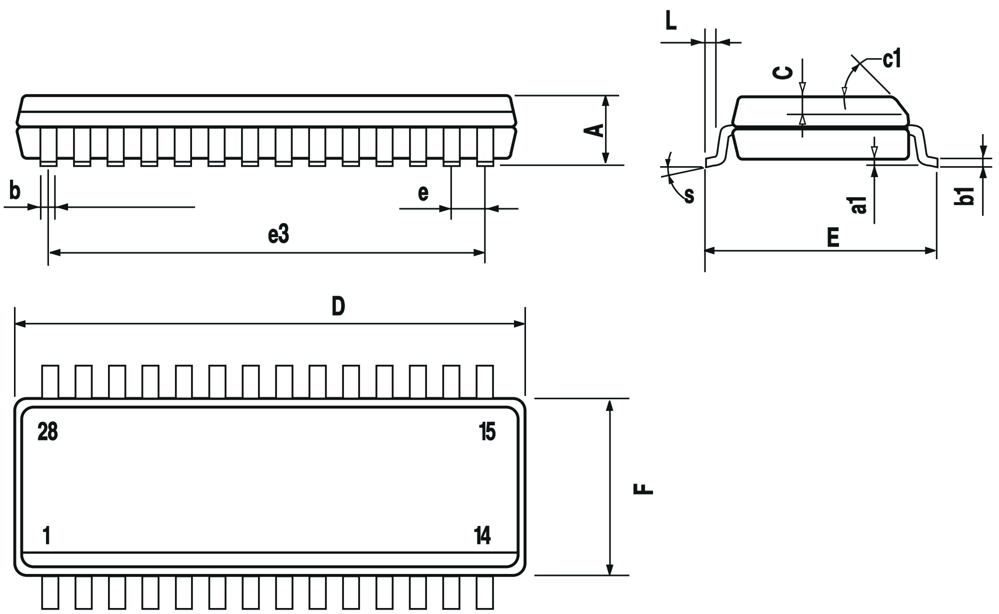
Figure 19. SO28 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28



10 REVISION HISTORY

Table 16. Revision History

Date	Revision	Description of Changes
January 2004	1	First Issue in EDOCS DMS
June 2004	2	Changed the Style-sheet in compliance to the new “Corporate Technical Pubblications Design Guide”
March 2006	3	Updated figure 19 “SO28 Mechanical Data & Package Dimensions”
30-Apr-2010	4	Updated title and added environmental compliance statement for package